PATENT ABSTRACTS OF JAPAN

(11)Publication number : 06-318590
(43)Date of publication of application : 15.11.1994

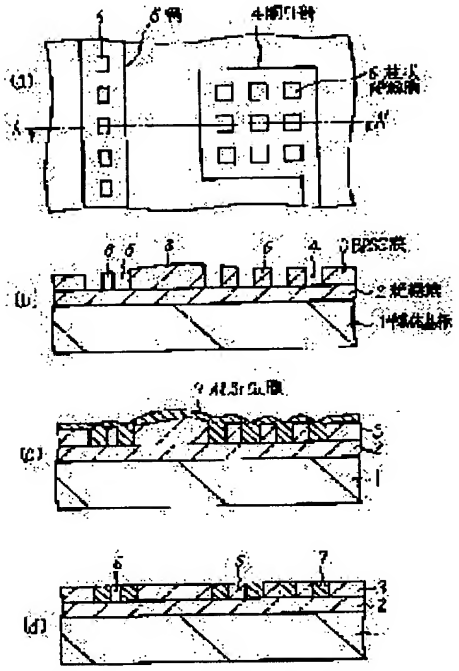
(51)Int.Cl. H01L 21/3205
H01L 21/304
// H01L 21/203

(21)Application number : 05-107805
(22)Date of filing : 10.05.1993

(71)Applicant : NEC CORP
(72)Inventor : HIRAKI MITSUMASA

(54) MANUFACTURE OF SEMICONDUCTOR DEVICE

(57)Abstract:
PURPOSE: To prevent excessive grinding and discontinuity when the surface of a metal film buried in a wide trench is polished by a chemical and mechanical polishing method, and a buried wiring is formed.
CONSTITUTION: When a trench 5 for forming a wiring or an aperture part 4 for forming a bonding pad are formed by patterning a BPSG film, pillar type insulating films 6 which are left and arranged inside the trench 5 and the aperture part 4 by patterning are formed. Thereby excessive grinding of an AlSiCu film 7 buried in the trench 5 and an aperture part 4 by a chemical and mechanical polishing is prevented.



LEGAL STATUS

[Date of request for examination]	10.05.1993
[Date of sending the examiner's decision of rejection]	02.09.1997
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	2972484
[Date of registration]	27.08.1999
[Number of appeal against examiner's decision of rejection]	09-16700
[Date of requesting appeal against examiner's decision of rejection]	02.10.1997
[Date of extinction of right]	

Copyright (C); 1998,2003 Japan Patent Office

06-318590

MANUFACTURE OF SEMICONDUCTOR DEVICE

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.

3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]

[Claim 1] The process which forms the 2nd insulator layer on the 1st insulator layer prepared on the semi-conductor substrate, Said 2nd insulator layer is etched alternatively. Pillar-shaped inside or the process which forms the slot for wiring formation of the shape of a grid which arranged and left said 2nd insulator layer by which patterning was carried out to the shape of a slit, The manufacture approach of the semiconductor device characterized by including the process which deposits a metal membrane on a front face including said slot, and is filled up with said Mizouchi, and the process which grinds the top face of said metal membrane and the 2nd insulator layer by the chemical machinery grinding method, embeds said metal membrane at said Mizouchi, carries out flattening of the top face, and forms embedded wiring.

[Claim 2] The manufacture approach of the semiconductor device according to claim 1 which deposits a metal membrane by the elevated-temperature spatter or the spatter reflow method.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] Especially this invention relates to the manufacture approach of a semiconductor device of having embedding wiring, about the manufacture

approach of a semiconductor device.

[0002]

[Description of the Prior Art] The surface flattening technique by the chemical machinery grinding method is indicated by the 57th page as one of the manufacture approaches of a semiconductor device in a proceeding buoy and El S eye multi-level INTAKONEKUTO conference (Proceeding VLSI Multilevel Interconnect Conference) 1991 [the 296th page or] in semiconductor technology symposium proceeding (Semiconductor Technology Symposium Proceeding) 1991.

[0003] Drawing 4 (a) - (d) is the top view of a semiconductor chip and B-B' line sectional view which were shown in order of the process for explaining the manufacture approach of the conventional semiconductor device.

[0004] First, as shown in drawing 4 (a) and (b), on the insulator layer 2 formed on the semi-conductor substrate 1, patterning of the BPSG (Boro-Phospho-Silicate Glass) film 3 is formed and carried out to the thickness of 0.7 micrometers, and the opening 4 for bonding pad formation and the slot 5 for wiring formation are formed.

[0005] Next, as shown in drawing 4 (c), the aluminum film (it is described as the AlSiCu film below) 7 which contains Si and Cu by the elevated-temperature spatter is deposited on a front face including opening 4 and a slot 5 at the thickness of 1 micrometer, and it is filled up in opening 4 and a slot 5.

[0006] Next, after grinding the upper part of the AlSiCu film 7 and the BPSG film 3 until the thickness of the BPSG film 3 turns into thickness which is about 0.5 micrometers by the chemical machinery grinding method as shown in drawing 4 (d), a silicon nitride film 8 is deposited on the thickness of 1.5 micrometers by the plasma-CVD method, patterning is carried out to the whole surface and the bonding pad section 9 and the embedded wiring 10 are formed in it.

[0007]

[Problem(s) to be Solved by the Invention] There was a problem that grinding is superfluously carried out in the center section of the slot by chemical machinery polish or opening, it becomes thin or disappears, junction on an open circuit of wiring, or a bonding pad and a bonding line cannot become imperfect, or the metal membrane filled up with the manufacture approach of this conventional semiconductor device into opening of a large area like large wiring of width of face or the bonding pad section could not join when the worst.

[0008]

[Means for Solving the Problem] The process which forms the 2nd insulator layer on the 1st insulator layer which established the manufacture approach of the

semiconductor device of this invention on the semi-conductor substrate, Said 2nd insulator layer is etched alternatively. Pillar-shaped inside or the process which forms the slot for wiring formation of the shape of a grid which arranged and left said 2nd insulator layer by which patterning was carried out to the shape of a slit, It is constituted including the process which deposits a metal membrane on a front face including said slot, and is filled up with said Mizouchi, and the process which grinds the top face of said metal membrane and the 2nd insulator layer by the chemical machinery grinding method, embeds said metal membrane at said Mizouchi, carries out flattening of the top face, and forms embedded wiring.

[0009]

[Example] Next, this invention is explained with reference to a drawing.

[0010] Drawing 1 (a) - (d) and drawing 2 (a), and (b) are the top views of a semiconductor chip and A-A' line sectional views which were shown in order of the process for explaining the 1st example of this invention.

[0011] First, as shown in drawing 1 (a) and (b), patterning of the BPSG film 3 is formed and carried out to the thickness of 0.7 micrometers on the insulator layer 2 formed on the semi-conductor substrate 1, and each of the opening 4 for bonding pad formation which arranged and left the pillar-shaped (shape of or slit) insulator layer 6, and the slot 5 for wiring formation is formed in the interior.

[0012] Next, as shown in drawing 1 (c), the AlSiCu film 7 is deposited on a front face including opening 4 and a slot 5 by the elevated-temperature spatter or the spatter reflow method, and it is filled up in opening 4 and a slot 5.

[0013] Next, as shown in drawing 1 (d), the top face of the AlSiCu film 7 and the BPSG film 3 is ground using the chemical machinery grinding method, and it grinds so that the thickness of the BPSG film 3 may be set to about 0.5 micrometers, and flattening of the pad front face is carried out for the AlSiCu film 7 into opening 4 and a slot 5.

[0014] Next, as shown in drawing 2 (a), a silicon nitride film 8 is deposited on the whole surface as a protective coat by the plasma-CVD method at the thickness of 1.5 micrometers.

[0015] Next, as shown in drawing 2 (b), a silicon nitride film 8 is etched alternatively and the bonding pad section 9 and the embedded wiring 10 are formed.

[0016] Thus, the superfluous grinding by chemical machinery polish can be prevented by preparing a pillar-shaped (shape of or slit) insulator layer beforehand for opening for pad formation with a large opening area, and Mizouchi for wiring formation, and subdividing opening.

[0017] Drawing 3 is the sectional view of the semiconductor chip for explaining the 2nd

example of this invention.

[0018] As shown in drawing 3 , after carrying out opening of the silicon nitride film 8 and forming the bonding pad section 9, by etching about 0.05 micrometers of front faces of the BPSG film 3 using buffered fluoric acid, and making the upper limit of the AlSiCu film 7 project further, the plane-of-composition product of the bonding pad section and a bonding line can be increased, and the bonding strength of a bonding line is raised.

[0019]

[Effect of the Invention] the superfluous grinding at the time of carry out chemical machinery polish and carry out flattening of the top face of the metal membrane for wiring with which Mizouchi be filled up by this invention arrange and prepare a column-like insulator layer for Mizouchi who formed in the embedded wiring formation with width of face wide at least as explain above, and subdivide the pattern of a slot be stop, poor junction of an open circuit of wiring, or a bonding pad and a bonding line prevent, and it have the effectiveness raise dependability.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The top view and A-A' line sectional view of a semiconductor chip which were shown in order of the process for explaining the 1st example of this invention.

[Drawing 2] The top view and A-A' line sectional view of a semiconductor chip which were shown in order of the process for explaining the 1st example of this invention.

[Drawing 3] The top view and B-B' line sectional view of a semiconductor chip which were shown in order of the process for explaining the manufacture approach of the conventional semiconductor device.

[Description of Notations]

1 Semi-conductor Substrate

2 Insulator Layer

3 BPSG Film

4 Opening

5 Slot

6 Pillar-shaped Insulator Layer

7 AlSiCu Film

8 Silicon Nitride Film

9 Bonding Pad Section
10 Embedded Wiring

Abstract:

PURPOSE: To prevent excessive grinding and discontinuity when the surface of a metal film buried in a wide trench is polished by a chemical and mechanical polishing method, and a buried wiring is formed.

CONSTITUTION: When a trench 5 for forming a wiring or an aperture part 4 for forming a bonding pad are formed by patterning a BPSG film, pillar type insulating films 6 which are left and arranged inside the trench 5 and the aperture part 4 by patterning are formed. Thereby excessive grinding of an AlSiCu film 7 buried in the trench 5 and an aperture part 4 by a chemical and mechanical polishing is prevented.

[Translation done.]

(19)日本国特許庁（ＪＰ）　(12) **公開特許公報**（Ａ）　(11)特許出願公開番号

特開平6－318590

(43)公開日　平成６年(1994)11月15日

(51)Int.Cl.[5]		識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ	21/3205				
	21/304	３２１　Ｓ	8832－4M		
// Ｈ０１Ｌ	21/203	Ｓ	8122－4M		
			7514－4M	Ｈ０１Ｌ　21/ 88	Ｋ

審査請求　有　　請求項の数２　ＯＬ　（全　３　頁）

(21)出願番号　特願平5－107805

(22)出願日　平成５年(1993)５月10日

(71)出願人　000004237
日本電気株式会社
東京都港区芝五丁目７番１号

(72)発明者　平木　光政
東京都港区芝五丁目７番１号日本電気株式会社内

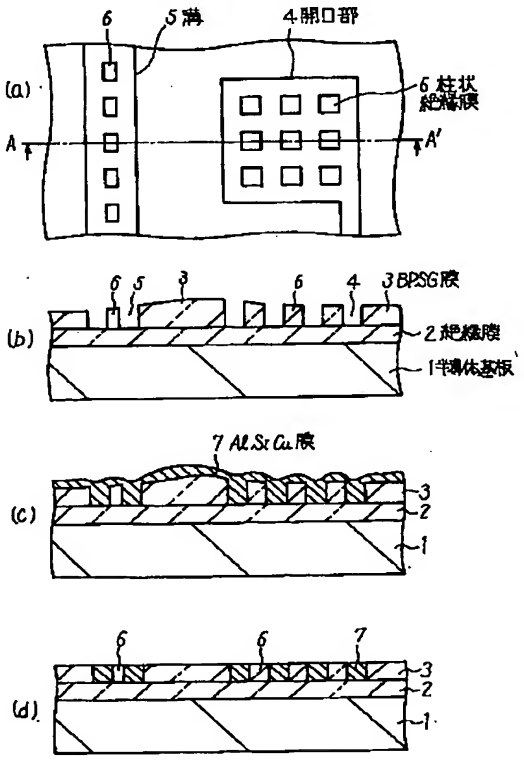
(74)代理人　弁理士　京本　直樹　（外２名）

(54)【発明の名称】　半導体装置の製造方法

(57)【要約】

【目的】幅の広い溝に充填した金属膜の表面を化学機械研磨法で研磨し埋込配線を形成する際の過剰研削を防ぎ断線を防止する。

【構成】ＢＰＳＧ膜をパターニングして配線形成用の溝５やボンディングパッド形成用の開口部４を形成する際にその内側にパターニングにより残して配列した柱状絶縁膜６を設けることにより溝５や開口部４に充填したＡＩＳｉＣｕ膜７の化学機械研磨による過剰研削を防止する。



【特許請求の範囲】

【請求項１】　半導体基板上に設けた第１の絶縁膜の上に第２の絶縁膜を形成する工程と、前記第２の絶縁膜を選択的にエッチングして内部に柱状又はスリット状にパターニングされた前記第２の絶縁膜を配列して残した格子状の配線形成用溝を形成する工程と、前記溝を含む表面に金属膜を堆積して前記溝内を充填する工程と、前記金属膜および第２の絶縁膜の上面を化学機械研磨法により研磨して前記溝内に前記金属膜を埋込んで上面を平坦化し埋込配線を形成する工程とを含むことを特徴とする半導体装置の製造方法。

【請求項２】　金属膜を高温スパッタ法又はスパッタリフロー法により堆積する請求項１記載の半導体装置の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明は半導体装置の製造方法に関し、特に埋め込み配線を有する半導体装置の製造方法に関する。

【０００２】

【従来の技術】半導体装置の製造方法の一つとして化学機械研磨法による表面平坦化技術がセミコンダクター・テクノロジィ・シンポジウム・プロシーディング（Ｓｅｍｉｃｏｎｄｕｃｔｏｒ　Ｔｅｃｈｎｏｌｏｇｙ　Ｓｙｍｐｏｓｉｕｍ　Ｐｒｏｃｅｅｄｉｎｇ）１９９１年、第２９６頁又はプロシーディング・ブイ・エル・エス・アイ・マルチレベル・インターコネクト・カンファレンス（Ｐｒｏｃｅｅｄｉｎｇ　ＶＬＳＩ　Ｍｕｌｔｉｌｅｖｅｌ　Ｉｎｔｅｒｃｏｎｎｅｃｔ　Ｃｏｎｆｅｒｅｎｃｅ）１９９１年、第５７頁に記載されている。

【０００３】図４（ａ）～（ｄ）は従来の半導体装置の製造方法を説明するための工程順に示した半導体チップの平面図およびＢ－Ｂ′線断面図である。

【０００４】まず、図４（ａ），（ｂ）に示すように、半導体基板１の上に形成した絶縁膜２の上にＢＰＳＧ（Ｂｏｒｏ－Ｐｈｏｓｐｈｏ－Ｓｉｌｉｃａｔｅ　Ｇｌａｓｓ）膜３を０．７μｍの厚さに成膜してパターニングし、ボンディングパッド形成用の開口部４および配線形成用の溝５を形成する。

【０００５】次に、図４（ｃ）に示すように、開口部４および溝５を含む表面に高温スパッタ法によりＳｉおよびＣｕを含むＡｌ膜（以下ＡｌＳｉＣｕ膜と記す）７を１μｍの厚さに堆積して開口部４および溝５内に充填する。

【０００６】次に、図４（ｄ）に示すように、ＡｌＳｉＣｕ膜７およびＢＰＳＧ膜３の上部を化学機械研磨法でＢＰＳＧ膜３の厚さが０．５μｍ程度の厚さになるまで研磨した後、全面にプラズマＣＶＤ法により窒化シリコン膜８を１．５μｍの厚さに堆積してパターニングし、ボンディングパッド部９および埋込配線１０を形成する。

【０００７】

【発明が解決しようとする課題】この従来の半導体装置の製造方法では、幅の広い配線やボンディングパッド部のように広い面積の開口部に充填された金属膜が化学機械研磨による溝や開口部の中央部で過剰に研削されて薄くなったり、あるいは消失したりして配線の断線やボンディングパッドとボンディング線との接合が不完全になったり、最悪の場合には接合できないという問題があった。

【０００８】

【課題を解決するための手段】本発明の半導体装置の製造方法は、半導体基板上に設けた第１の絶縁膜の上に第２の絶縁膜を形成する工程と、前記第２の絶縁膜を選択的にエッチングして内部に柱状又はスリット状にパターニングされた前記第２の絶縁膜を配列して残した格子状の配線形成用溝を形成する工程と、前記溝を含む表面に金属膜を堆積して前記溝内を充填する工程と、前記金属膜および第２の絶縁膜の上面を化学機械研磨法により研磨して前記溝内に前記金属膜を埋込んで上面を平坦化し埋込配線を形成する工程とを含んで構成される。

【０００９】

【実施例】次に、本発明について図面を参照して説明する。

【００１０】図１（ａ）～（ｄ）および図２（ａ），（ｂ）は本発明の第１の実施例を説明するための工程順に示した半導体チップの平面図およびＡ－Ａ′線断面図である。

【００１１】まず、図１（ａ），（ｂ）に示すように、半導体基板１の上に形成した絶縁膜２の上にＢＰＳＧ膜３を０．７μｍの厚さに形成してパターニングし、内部に柱状（又はスリット状）絶縁膜６を配列して残したボンディングパッド形成用の開口部４および配線形成用の溝５のそれぞれを形成する。

【００１２】次に、図１（ｃ）に示すように、開口部４および溝５を含む表面に高温スパッタ法又はスパッタリフロー法によりＡｌＳｉＣｕ膜７を堆積して開口部４および溝５内に充填する。

【００１３】次に、図１（ｄ）に示すように、化学機械研磨法を用いてＡｌＳｉＣｕ膜７およびＢＰＳＧ膜３の上面を研磨し、ＢＰＳＧ膜３の厚さが０．５μｍ程度になるように研磨して開口部４および溝５内にＡｌＳｉＣｕ膜７を埋込み表面を平坦化する。

【００１４】次に、図２（ａ）に示すように、全面にプラズマＣＶＤ法により保護膜として窒化シリコン膜８を１．５μｍの厚さに堆積する。

【００１５】次に、図２（ｂ）に示すように、窒化シリコン膜８を選択的にエッチングしてボンディングパッド部９および埋込配線１０を形成する。

【００１６】このように、開口面積の広いパッド形成用

開口部や配線形成用溝内に予め柱状（又はスリット状）絶縁膜を設けて開口部を細分化することにより化学機械研磨による過剰な研削を防止することができる。

【００１７】図３は本発明の第２の実施例を説明するための半導体チップの断面図である。

【００１８】図３に示すように、窒化シリコン膜８を開口してボンディングパッド部９を形成した後、更に、バッファードフッ酸を用いＢＰＳＧ膜３の表面を０．０５μｍ程度エッチングしてＡｌＳｉＣｕ膜７の上端を突出させることにより、ボンディングパッド部とボンディング線との接合面積を増大させることができ、ボンディング線の接合強度を向上させる。

【００１９】

【発明の効果】以上説明したように本発明は、少くとも幅の広い埋込配線形成用に形成した溝内に柱状の絶縁膜を配列して設け溝のパターンを細分化することにより、溝内に充填した配線用金属膜の上面を化学機械研磨して平坦化する際の過剰な研削を抑えて配線の断線やボンディングパッドとボンディング線との接合不良を防止し、信頼性を向上させるという効果を有する。

【図面の簡単な説明】

【図１】本発明の第１の実施例を説明するための工程順に示した半導体チップの平面図およびＡ－Ａ′線断面図。

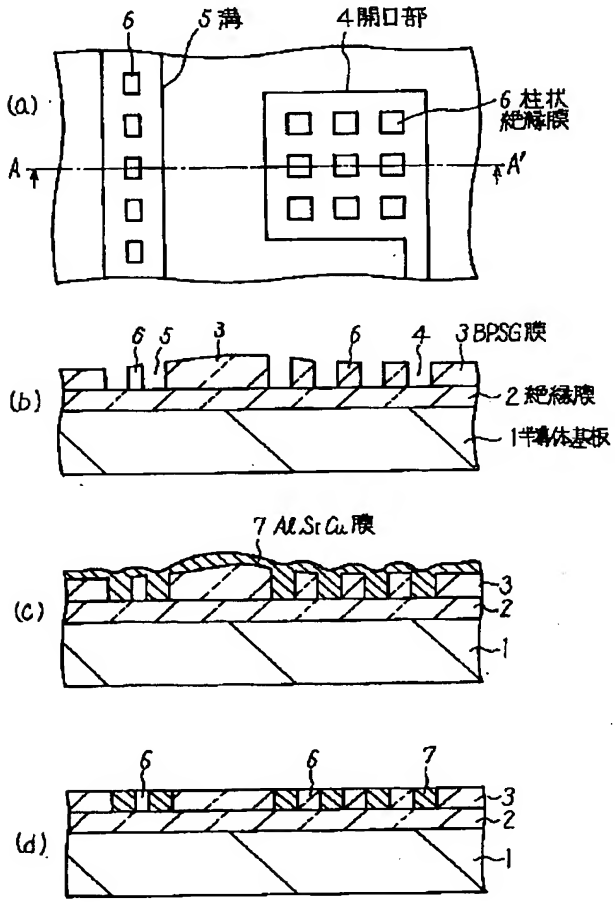
【図２】本発明の第１の実施例を説明するための工程順に示した半導体チップの平面図およびＡ－Ａ′線断面図。

【図３】従来の半導体装置の製造方法を説明するための工程順に示した半導体チップの平面図およびＢ－Ｂ′線断面図。

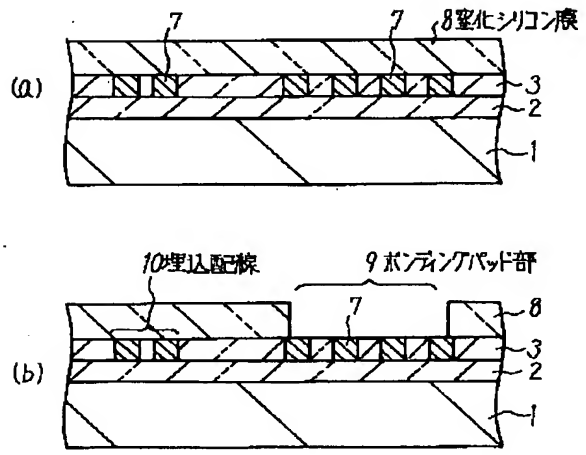
【符号の説明】

１	半導体基板
２	絶縁膜
３	ＢＰＳＧ膜
４	開口部
５	溝
６	柱状絶縁膜
７	ＡｌＳｉＣｕ膜
８	窒化シリコン膜
９	ボンディングパッド部
１０	埋込配線

【図１】



【図２】



【図３】